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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,153	MORAN, DOV	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-30 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-30 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed March 22, 2004 in response to PTO Office Action mailed January 28, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1, 3-30 and 36 have been presented for examination in this application. In response to the last Office Action, no claims have been amended. No claims have been canceled. Claim 36 has been added. As a result, claims 1, 3-30 and 36 are now pending in this application.

3. The rejection of claims 1 and 3-30 as in the Office action mailed January 28, 2004 (Paper No. 14) is respectfully maintained and reiterated below for applicant's convenience.

Claim Objections

4. Claim 3 is objected to because of the following informalities:

It appears that in claim 3, line 1, "claim 2" should be changed to –claim 1--. The dependency of claim 3 on claim 2 is erroneous since claim 2 has been canceled.

Appropriate correction is required.

Response to Arguments

5. Applicant's arguments filed March 22, 2004 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

(a) Garfunkel's flash memory is executable.

Examiner respectfully traverses applicant's arguments for the following reasons.

Examiner would like to point out that nowhere in Garfunkel does the reference disclose that code is executed from the flash. Because the reference teaches that during updating, controller 11 operates a section of the program from the RAM 13, rather than from the flash memory as detailed in column 7, lines 1-3, does not necessarily mean that code is executed from flash in other circumstances. Examiner would like to pint out that during initialization, which occurs when the system power-up, program is copied in the RAM and the initialization process continues from the RAM (see column 7, lines 24-38). Thus, it can be clearly seen that when the system boots, the boot code is also ran from the RAM in a manner similar as that claimed by applicant.

(b) There is no hint or suggestion of special circuitry analogous to applicant's logic 42, separate from controller 11, in the system of Garfunkel for copying boot code from sector 21 of flash memory 12 to RAM 13 on power-up.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *a special circuitry analogous to applicant's logic 42, separate from controller 11*, in

the system of Garfunkel for copying boot code from sector 21 of flash memory 12 to RAM 13 on power-up) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Examiner would suggest that applicant amend the claims to more clearly point out the subject matter which applicant sees as his invention and to further differentiate from the prior art of record.

(c) The prior art of record does not teach or suggest how volatile memory is coupled to flash memory.

Examiner respectfully traverses applicant's arguments for the following reasons. The invention as claimed provides for a first bus providing communication between an external processor and a flash based unit and a second bus separate from the first bus to move code from the flash memory to the volatile memory. Although Brown discloses a processor 100 coupled to a flash unit by a first bus, Brown does not disclose a second bus. However, as detailed in the previous Office Action, Kakinuma discloses a first bus coupling the processor 1 to flash memory 4 (primary bus in Fig. 3) and a second bus separate from the first bus to move code from the flash memory to the volatile memory (bus coupling buffer memory 3 to flash memory 4 through buffer memory manager 6; Fig. 3). It can be clearly seen that Kakinuma discloses the coupling of the flash memory, the processor, the volatile memory and the busses in a manner similar as that claimed by applicant.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Examiner would suggest that applicant amend the claims to include for instance that the second bus is an internal bus" to more clearly point out the subject matter which applicant sees as his invention and clearly distinguish his invention from the prior art of record.

(d) Kakinuma use buffer memories 22 and 23 only to buffer data between flash memories 20 and 21 and host computer 1.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to point out that Kakinuma the use of a buffer memory 3 (S-RAM) to present code to the processor or host for execution as claimed by applicant.

(e) In claim 19 and 36, although Garfunkel and Chieng both disclose an embedded system, they also disclose that their invention can be carried out using an external microcontroller or a microprocessor or host processor to control the operation of the embedded system (see Garfunkel, col. 7, lines 62-66 and Chieng, col. 4, lines 56-62).

(f) The volatile memory component, not the flash memory that is large enough to store the basic initialization code.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to point out that Lee discloses that by using a RAM or volatile memory of a small capacity, the correction and maintenance of the codes are easy and multiple functions are obtained (see column 4, lines 24-29). Thus, it can be clearly seen that the volatile memory being 32k words is large enough to store 8k words and does not constitute the novelty of applicant's invention.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 22 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Garfunkel et al (US6,615,404).

As per claim 22, Garfunkel discloses a method for booting a system, the system featuring a processor for executing boot code, the method comprising:

providing a flash based unit in the system for storing the boot code to be executed [*flash memory 12 stores boot instructions*; col. 5, lines 12-15], said flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot

be directly executed from said flash memory [*software can not be run form the flash memory 12*; col. 7, lines 5-8], and a volatile memory component for receiving a portion of the boot code to be executed [*boot segment is copied in RAM 13*; col. 7, lines 27-30], said portion of the boot code being for basic initialization of the system and containing a command for copying a second portion of the code [*initialization continues from RAM*; *a new downloading and programming process is enabled*; col. 7, lines 27-38]; executing said first portion of the boot code by said processor to boot the system [*the RAM enables the controller to operate the system*; col. 4, lines 46-52].

As per claim 23, Garfunkel discloses transferring a second portion of the code to said volatile memory component for booting the system [col. 7, lines 27-38].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 10-13, 16-18, 20-21 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Kakinuma et al (US5,640,349) and further in view of Garner (US6,549,482).

As per claims 1, 12, 18, 20 and 21, Brown discloses a flash-based unit for providing code to be executed by an external processor that is in communication with the flash based unit by a first bus, the flash based unit comprising a flash memory for storing the code to be executed [*flash EPROM stores both code and data;* col. 9, line 50], said flash memory being of a type such that the code cannot be executed in place from said flash memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-33]; a volatile memory component for receiving at least a portion of the code to be executed, such that at least said portion of the code is executed by the external processor from said volatile memory component [*the code of the flash memory is copied to volatile memory where the processor can satisfy the code fetch request;* col. 4, lines 4-8].

However, although Brown discloses that the volatile memory and the flash EPROM could be coupled to the processor via separate buses [col. 3, lines 64-65], the reference does not specifically teach a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component; and a second bus, separate from said first bus, whereby said logic moves said at least portion of the code from said flash memory to said volatile memory component; and that a processor could execute code resident in volatile memory as recited in the claims.

Kakinuma discloses a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component [*flash memory controller 2 controls read/write to/from flash memory based on command by host computer;* Fig. 3, col. 1, line 35 – col. 2, line 3]; and a second bus,

separate from said first bus, whereby said logic moves said at least portion of the code from said flash memory to said volatile memory component [*note that the flash memory 4 communicates with S-RAM 3 and host 1 through a separate bus*; Fig. 3].

Garner discloses a processor could execute code resident in volatile memory [*the code can be executed from RAM*; col. 2, lines 30-34].

It would have been obvious to one of ordinary skill in the art, having the teachings of Brown and Kakinuma and Garner before him at the time the invention was made, to modify the system of Brown to include a logic, separate from the external processor, and a separate bus for communication between the flash memory and the volatile memory because a separate logic functions to control write/read operation to/from a flash memory based upon a command by a host processor (Kakinuma, col. 1, lines 35-37); using a separate bus is well known to benefit by improving system throughput; and executing code resident in volatile memory is well known to benefit by allowing the processor to perform an executable command instruction to the flash device while reading the code from RAM (Garner, col. 2, lines 36-37).

As per claims 10 and 16, Brown discloses a volatile memory component selected from the group consisting of SRAM or DRAM [col. 4, lines 1-3].

As per claim 11 and 17, Garner discloses the initialization code is boot code [col. 2, lines 38-42].

As per claim 13, Brown discloses a restricted non-volatile memory is a flash memory [col. 5, lines 30-32].

As per claims 29 and 30, Brown discloses a port for providing to the external processor said at least portion of the code received by said volatile memory component [*port located between host computer 1 and host computer interface control 5*; Fig.3].

10. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Kakinuma et al (US5,640,349) and further in view of Garner (US6,549,482) and Anderson et al (US6,295,577).

As per claim 3, the combination of Brown and Kakinuma and Garner discloses the claimed invention as detailed above in the previous paragraphs. However, Brown and Kakinuma and Garner do not specifically teach a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available as recited in the claim.

Anderson discloses a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available [*power is supplied to the non-volatile memory upon loss of power;* col. 6, lines 2-6].

As per claim 4, the combination of Brown and Kakinuma and Garner discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Brown and Kakinuma and Garner does not specifically teach a power

storage providing only sufficient power to write data in said volatile memory to said flash memory as recited in the claim.

Anderson discloses a power storage providing only sufficient power to write data in said volatile memory to said flash memory [*data is stored from volatile memory to non-volatile memory upon detection of loss of power;* col. 5, lines 61-67].

As per claim 5, the combination of Brown and Kakinuma and Garner discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Brown and Kakinuma and Garner does not specifically teach the power storage is a capacitor as recited in the claim.

Anderson discloses the power storage is a capacitor [col. 3, lines 62-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of the combination of Brown and Kakinuma and Garner and Anderson before him at the time the invention was made, to modify the system of Brown and Kakinuma and Garner to include a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available; a power storage providing only sufficient power to write data in said volatile memory to said flash memory and the power storage is a capacitor because it would have decreased system cost by using a back EMF to power the non-volatile memory rather than battery based systems [col. 5, lines 10-14] as taught by Anderson.

11. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Kakinuma et al (US5,640,349) and further in view of Garner (US6,549,482) and Mills et al (US6,385,688).

As per claims 6 and 7, the combination of Brown and Kakinuma and Garner discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Brown and Kakinuma and Garner does not specifically teach a single chip or die for containing all components of a flash based unit as recited in the claims.

Mills discloses a single chip or die for containing all components of a flash based unit [col. 20, lines 1-4].

It would have been obvious to one of ordinary skill in the art, having the teachings of the combination of Brown and Kakinuma and Garner and Mills before him at the time the invention was made, to modify the system of the combination of Brown and Kakinuma and Garner to include a single chip or die for containing all components of a flash based unit because it would have improved system performance by reducing or eliminating the lengthy process of obtaining information from disk when power is turned on [col. 9, lines 15-20] as taught by Mills.

12. Claims 8-9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Kakinuma et al (US5,640,349) and further in view of Garner (US6,549,482) and Nakata (US6,523,101).

As per claims 8 and 14, the combination of Brown and Kakinuma and Garner discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Brown and Kakinuma and Garner does not specifically teach a flash memory only permitting data to be read in one or more specific sizes of blocks as recited in the claim.

Nakata discloses a flash memory only permitting data to be read in one or more specific sizes of blocks [*ROM indicates copy size of initialization data to be stored into RAM;* col. 3, lines 41-44].

It would have been obvious to one of ordinary skill in the art, having the teachings of the combination of Brown and Kakinuma and Garner and Nakata before him at the time the invention was made, to modify the system of the combination of Brown and Kakinuma and Garner to include a flash memory only permitting data to be read in one or more specific sizes of blocks because it would have increased execution speed of the program by allowing the text codes stored on the ROM to be copied once into the RAM [col. 1, lines 43-46] as taught by Nakata.

As per claims 9 and 15, Brown discloses a flash memory is a NAND-type flash memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-33].

13. Claims 19 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garfunkel et al (US6,615,404) and Chieng et al (US6,035,346).

As per claims 19, Garfunkel discloses a method for booting a system, the system featuring a processor for executing boot code, the method comprising:

providing a flash based unit in the system for storing the boot code to be executed [col. 5, lines 12-15], said flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot be directly executed from said flash memory [col. 7, lines 5-8], and a volatile memory component for receiving a portion of the boot code to be executed [col. 7, lines 27-30], said portion of the boot code being for basic initialization of the system [col. 7, lines 27-32];

However, Garfunkel does not specifically teach sending a busy signal to said processor; transferring said portion of the boot code to said volatile memory component; removing said busy signal; and executing the portion of the code to boot the system as recited in the claim.

Chieng discloses sending a busy signal to said processor [col. 3, lines 33-35]; transferring said portion of the boot code to said volatile memory component [col. 3, lines 36-39]; removing said busy signal [col. 3, lines 42-44]; and executing the portion of the code to boot the system [col. 3, lines 45-49].

Since the use of a busy state is well known, and since a busy state prevents reprogramming instruction errors, an artisan would have been motivated to implement a busy state in the system of Garfunkel. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Garfunkel and Chieng before him at the

time the invention was made, to modify the system of Garfunkel to use a busy state because a busy state is well known to benefit by preventing reprogramming instruction errors.

As per claim 36, Garfunkel discloses a flash-based unit separate from the processor [*flash memory 12 is separate from processor coupled to comm. link 14*; Fig. 1; col. 7, lines 62-66].

14. Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garfunkel et al (US6,615,404) and Lee (US6,370,645)

As per claims 24-28, Garfunkel discloses the claimed invention as detailed per claim 22 above in the previous paragraphs. However, Garfunkel does not specifically teach that the volatile memory is large enough to store portion of the boot code only sufficient for basic initialization of a system as recited in the claims.

Lee discloses the use of a volatile memory is large enough to store at least portion of a boot code only sufficient for basic initialization of a system to easily correct a bug and appropriately cope with the demand for upgrading in relation to the process test, reliability and compatibility [col. 2, lines 16-20; col. 3, line 49 – col. 4, line 29]. Since a volatile memory is large enough to store at least portion of a boot code only sufficient

for basic initialization of a system benefits by easily correcting a bug and appropriately coping with the demand for upgrading in relation to the process test, reliability and compatibility, an artisan would have been motivated to implement a volatile memory is large enough to store at least portion of a boot code only sufficient for basic initialization of a system in the system of Garfunkel. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a volatile memory is large enough to store at least portion of a boot code only sufficient for basic initialization of a system because it was well known to benefit with easily correcting a bug and appropriately coping with the demand for upgrading in relation to the process test, reliability and compatibility as taught by Lee.

15. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US6,201,739) and Kakinuma et al (US5,640,349) and further in view of Garfunkel et al (US6,615,404).

As per claims 31-35, Brown discloses a flash-based unit for providing code to be executed by an external processor that is in communication with the flash based unit by bus, the flash based unit comprising a flash memory for storing the code to be executed [*flash EPROM stores both code and data;* col. 9, line 50], said flash memory being of a type

such that the code cannot be executed in place from said flash memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-33]; a volatile memory component for receiving at least a portion of the code to be executed, such that at least said portion of the code is executed by the external processor from said volatile memory component [*the code of the flash memory is copied to volatile memory where the processor can satisfy the code fetch request;* col. 4, lines 4-8].

However, Brown does not specifically teach a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component upon receipt of a power-on signal as recited in the claim.

Kakinuma discloses a logic, separate from the external processor, for receiving command to move said at least portion of the code from said flash memory to said volatile memory component [*flash memory controller 2 controls read/write to/from flash memory based on command by host computer*; Fig. 1A, 1B, col. 1, line 35 – col. 2, line 3]. Since the technology for implementing a logic separate from a processor for moving data was well known, and since a separate logic functions to control write/read operation to/from a flash memory based upon a command by a host processor, an artisan would have been motivated to implement a logic separate from a processor in the system of Brown.

However Kakinuma does not specifically teach the use of a power-on signal to move code data from said flash memory to said volatile memory component as recited in the claim.

Garfunkel discloses moving code data from a flash memory to a volatile memory component upon power-on [col. 5, lines 12-15]. Since the technology for implementing moving code data from a flash memory to a volatile memory component upon power-on was well known, and since moving code data from a flash memory to a volatile memory component upon power-on eliminates a situation where the flash memory contains only corrupted or incomplete software version, an artisan would have been motivated to implement moving code data from a flash memory to a volatile memory component upon power-on in the system of Brown and Kakinuma.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a logic separate from a processor for moving data, because a logic separate from a processor was well known to benefit by control write/read operation to/from a flash memory based upon a command by a host processor as taught by Kakinuma; and to move code data from a flash memory to a volatile memory component upon power-on, because move code data from a flash memory to a volatile memory component upon power-on was well known to benefit by eliminating a situation where the flash memory contains only corrupted or incomplete software version as taught by Garfunkel.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 3, 2004

Pierre M. Vital
Examiner
Art Unit 2188